REMARKS

Claims 1-22 are pending. In the Office Action, claims 5-8 were objected to because of informalities, claims 1, 9-14 and 19-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yer et al. (Yer, US 20020109655) in view of Tanaka et al. (Tanaka, US 20030132906), and claims 2-4 and 15-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yer in view of Tanaka and Suzuki et al. (Suzuki, US Pat. No. 6,157,335).

Claims 5-8 were objected to as being dependent upon a reject base claim (and because of informalities as noted above), but were otherwise considered allowable.

Paragraph 26 of the specification is amended to correct the spelling of the word "implementation". Applicant submits that this was an inadvertent spelling error and that correction does not add new matter. Applicant requests approval of this amendment.

Claims 5-8 were objected to because of informalities. In particular, the value "Q" was stated as being undefined in claim 5. It is noted that a value "M" is recited in claim 1 with reference to "adjustable tap resistors" and "tap voltages" and it is apparent from the claim text that M is a number. Similarly, a value "P" is recited in claim 2 with reference to "resistors" and "intermediate junctions" and it is also apparent from the claim text that P is a number. In each case, M and P are referred to as comprising "a positive integer." Also, a value "Q" is recited in claim 5 with reference to "second resistors", "intermediate locations" and "switch sets" and it is also apparent that Q is a number, although it is not stated as comprising a positive integer. Applicant respectfully submits that Q is actually defined sufficiently and that further specifying a number as a positive integer is

extraneous and/or unnecessary. Nonetheless, claim 5 is amended for consistency to refer to the value Q as a "positive integer" in a similar manner as the values M and P in prior claims as noted above. Applicant requests withdrawal of this objection.

Applicant respectfully traverses the §103(a) rejection of claims 1, 9-14 and 19-22 as being unpatentable over Yer in view of Tanaka.

Contrary to that stated on page 2 of the Office Action, Yer does not show a "resistor ladder including M adjustable tap resistors distributed along said resistor ladder" as recited in claim 1. Figures 1-7 of Yer describe a "related art" configuration. In FIG. 3 of Yer, the resistor ladders comprising resistors R1-R6 and R7-R12 include *fixed* resistors rather than *adjustable tap resistors*. The fixed resistors develop a "fixed gamma voltage" as shown by the gray curve of FIG. 6 and as described in paragraph [0035] of Yer. The problem of the related art luminance voltage characteristic of the related art described in Yer is that "the related art luminance voltage characteristic does not adapt to variation of peripheral luminous intensity and user's requests due to a gamma voltage being initially set according to the LCD module" (Yer, paragraph [0037]). The reason is that the related art luminance voltage characteristic described in Yer is fixed.

Yer further describes a programmable gamma voltage generator as shown in FIGs 8 and 9 of Yer. Yet Yer's programmable gamma voltage generator also does not show "resistor ladder including M adjustable tap resistors distributed along said resistor ladder" as recited in claim 1. As described in paragraph [0063] of Yer, the programmable gamma voltage generator 81 includes a digital variable resistor 81b which "adjusts *a resistance value* to correspond to mode information output from the memory 81a"

(emphasis added), in which "a gamma voltage outputting unit 81c outputs a plurality of gamma voltages GMA1-GMA10 corresponding to *the resistance value* adjusted by the digital variable resistor 81b to the source driver 89" (emphasis added). As further described in paragraph [0068] of Yer, "[t]he digital variable resistor 81b adjusts *a resistance value* for adjusting gamma voltages based on digital information corresponding to the peripheral environment information output from the memory 81a" (emphasis added). In other words, a single digital variable resistor is used in Yer's configuration to generate the plurality of gamma voltages. Yer's embodiment does not show "a resistor ladder including M adjustable tap resistors distributed along said resistor ladder" as recited in claim 1.

And further, since Yer does not employ a resistor ladder with adjustable tap resistors, Yer further does not show select logic which "selects a tap point of each of said M adjustable tap resistors to select each of said M tap voltages based on corresponding select values" as recited in claim 1 since there are not adjustable tap resistors in a resistor ladder in the first place. As described in paragraphs [0072-0073] of Yer, an environment sensor 83 senses a changed peripheral environment and outputs information about the current environment to a controller 85. The controller 85 designates an address of the memory 81a based on information input from the environment sensor 83. The memory 81a outputs digital information stored in the designated address, and the digital variable resistor 81b adjusts *a resistance value* to correspond to the digital information output from the memory 81a. The gamma voltages are determined at levels from GMA1 to GMA10 in accordance with *the adjusted resistance value*. So it appears from Yer's description that a single programmed resistance value is used to determine multiple

gamma voltage levels according to predetermined gamma curves as shown in FIG. 10 of Yer. Yer does not show a resistor ladder including M adjustable tap resistors distributed along the resistor ladder or select logic which selects a tap point of each of the M adjustable tap resistors to select each of M tap voltages based on corresponding select values as recited in claim 1.

Tanaka is cited for the limited teaching of an integrated circuit (see page 3 of Office Action). Otherwise, Tanaka fails to overcome the deficiencies of Yer, so that claim 1 is allowable over Yer in view of Tanaka. Tanaka also does not show a "resistor ladder including M adjustable tap resistors distributed along said resistor ladder" as recited in claim 1. Instead, Tanaka selects from among an array of weighted current sources as shown in FIG. 6 of Tanaka.

Applicant respectfully submits, therefore, that claim 1 is allowable over Yer in view of Tanaka. Claims 9-13 are allowable as depending upon allowable claim 1. Applicant requests withdrawal of this rejection.

Further with respect to claims 9 and 10, the memory 81a of Yer is only described as outputting digital information corresponding to a plurality of modes for different peripheral environments for adjusting the resistance value of the digital variable resistor 81b (Yer, paragraphs [0064-73]) and is not described as storing a "plurality of sets of select values ... for selecting from among said plurality of sets of select values and loading said set of latches" as recited in claim 9.

Claim 14 is allowable over Yer in view of Tanaka for similar reasons recited above with respect to claim 1. Yer in view of Tanaka does not show a resistor ladder

including "a plurality of adjustable tap resistors distributed along said resistor ladder and providing a plurality of selectable tap voltages" and "select logic … that selects each of said selectable tap voltages according to said at least one digital gamma value" as recited in claim 14.

Claim 19 is allowable over Yer in view of Tanaka for similar reasons recited above with respect to claim 1. Yer in view of Tanaka does not show a programmable gamma correction voltage generator including "a plurality of potentiometers distributed along" a resistor ladder as recited in claim 19. Yer in view of Tanaka further does not show "select logic … that selects each of said variable tap voltages according to said digital gamma value" as further recited in claim 19.

Applicant respectfully submits, therefore, that claim 19 is allowable over Yer in view of Tanaka. Claims 20-22 are allowable as depending upon allowable claim 19. Applicant requests withdrawal of this rejection.

Applicant respectfully traverses the §103(a) rejection of claims 2-4 and 15-18 as being unpatentable over Yer in view of Tanaka and Suzuki.

Suzuki does not overcome the deficiencies of Yer in view of Tanaka described above, so that claims 2-4 are allowable as depending upon allowable claim 1 and claims 15-18 are allowable as depending upon allowable claim 14. Applicant requests withdrawal of this rejection.

Further with respect to claims 16 and 17, Yer in view of Tanaka and Suzuki does not show a plurality of first resistors distributed along the resistor ladder in which each

first resistor comprises a plurality of second resistors coupled in series forming a plurality of first junctions and first switch logic that inserts a corresponding adjustable tap resistor at one of the plurality of first junctions of the first resistors as recited in claim 16. There is no showing or suggestion whatsoever of switch logic that selectively inserts adjustable tap resistors into one of a plurality of junctions of the second resistors as recited in claim 16. As described in Suzuki, (col. 6, lines 26-59 and FIGs 4 and 8), only one of the switches SW1-SW8 is turned on to select a corresponding potential Va to an input of the amplifier 25, which adjusts the current Ia for purposes of adjusting bias current through a resistor array.

None of the amendments made herein were related to the statutory requirements of patentability, but instead were made for purposes of clarity or consistency. Also, none of the amendments were made for the purpose of narrowing the scope of any claim.

CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the objections and rejections have been overcome and should be withdrawn. Applicant respectfully submits therefore that the present application is in a condition for allowance and reconsideration of the claims is respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference at (512) 295-8050.

Respectfully submitted,

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